



# Low-power Low-jitter Clock Distribution Network for LPDDR5

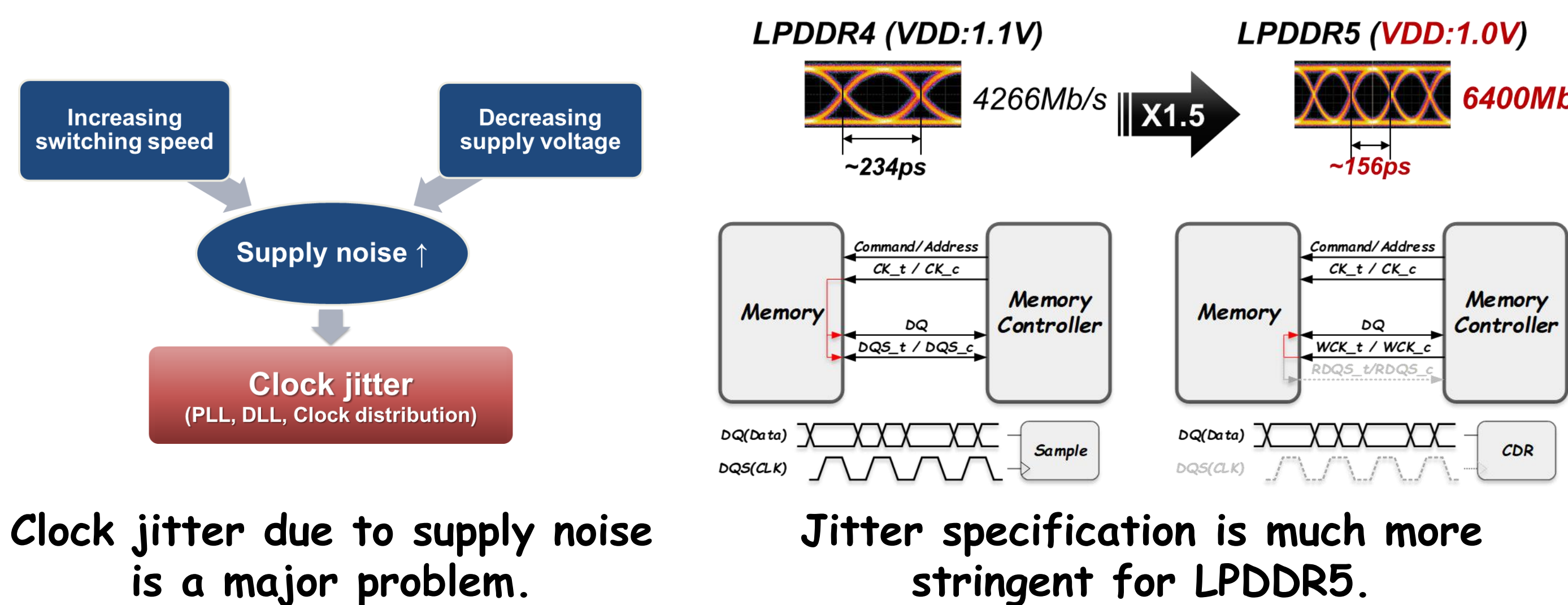
School of Electrical Engineering, KAIST

Seongseop Lee, SeongHwan Cho

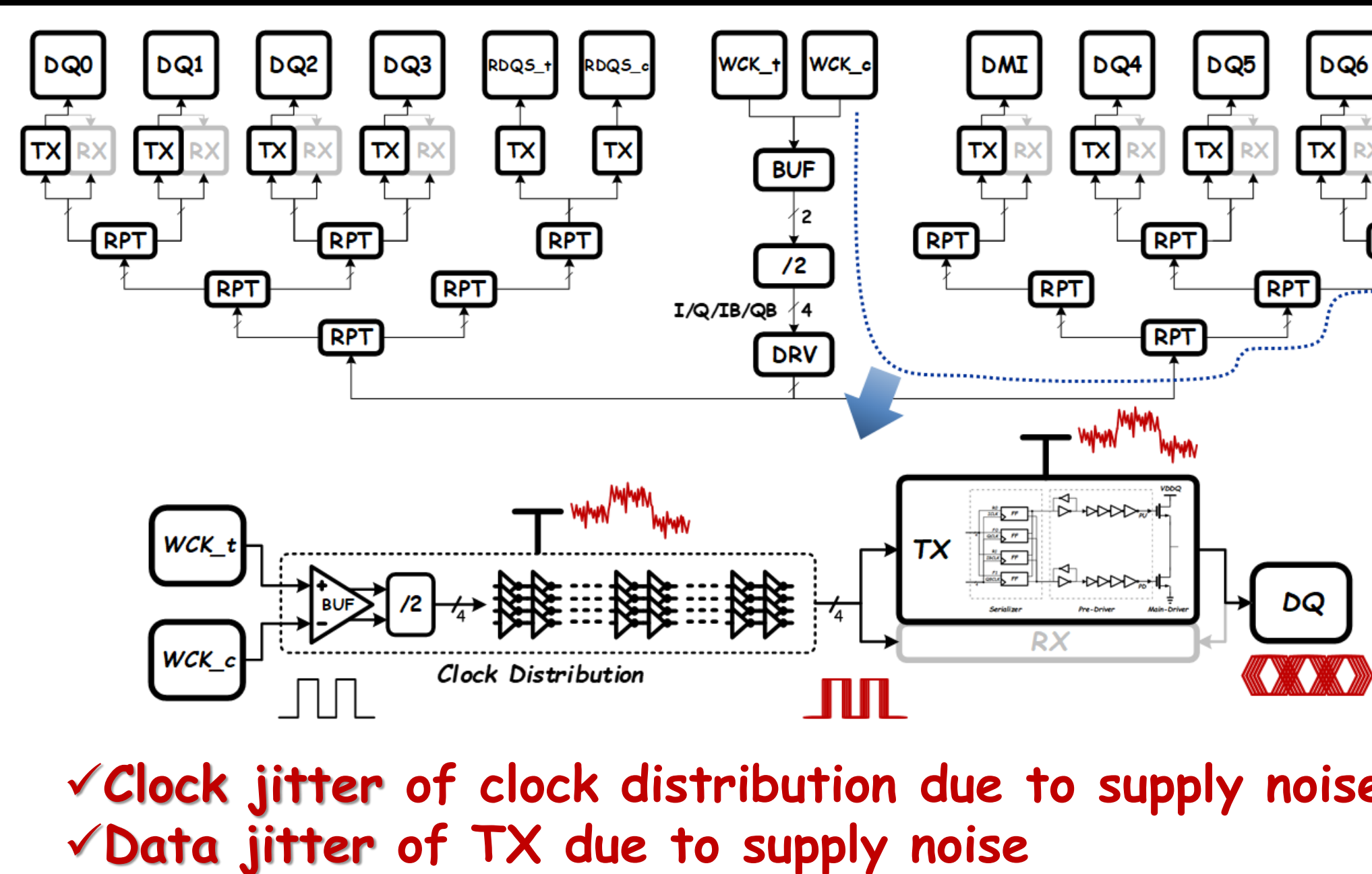
## Introduction

### Problem in Low Power & High Performance Device

The increased clock jitter caused by power supply noise reduces the timing margin of the internal circuitry, making high-performance operation difficult.

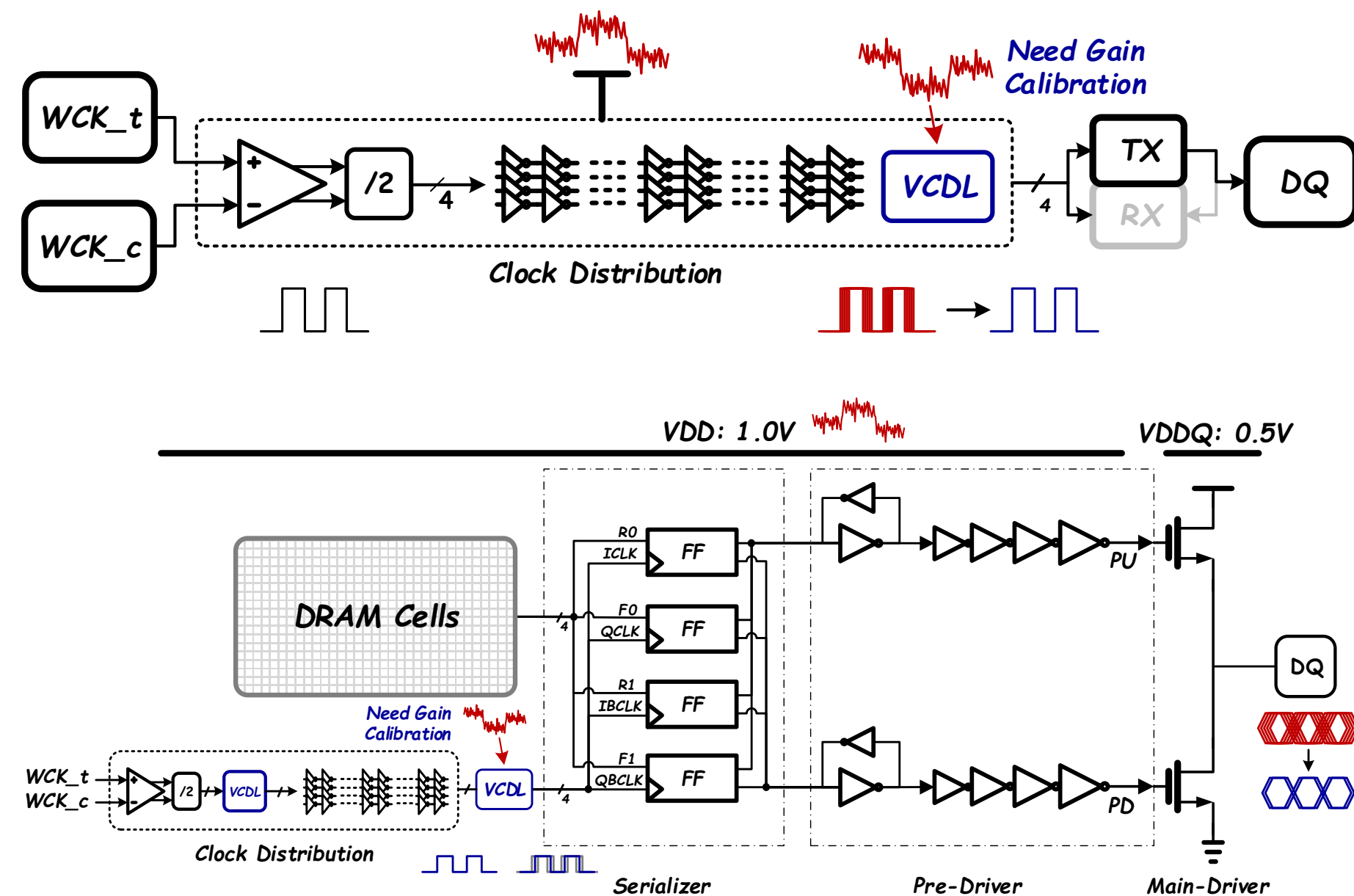


### Clock & Data Jitter Caused by Power Supply Noise in LPDDR5



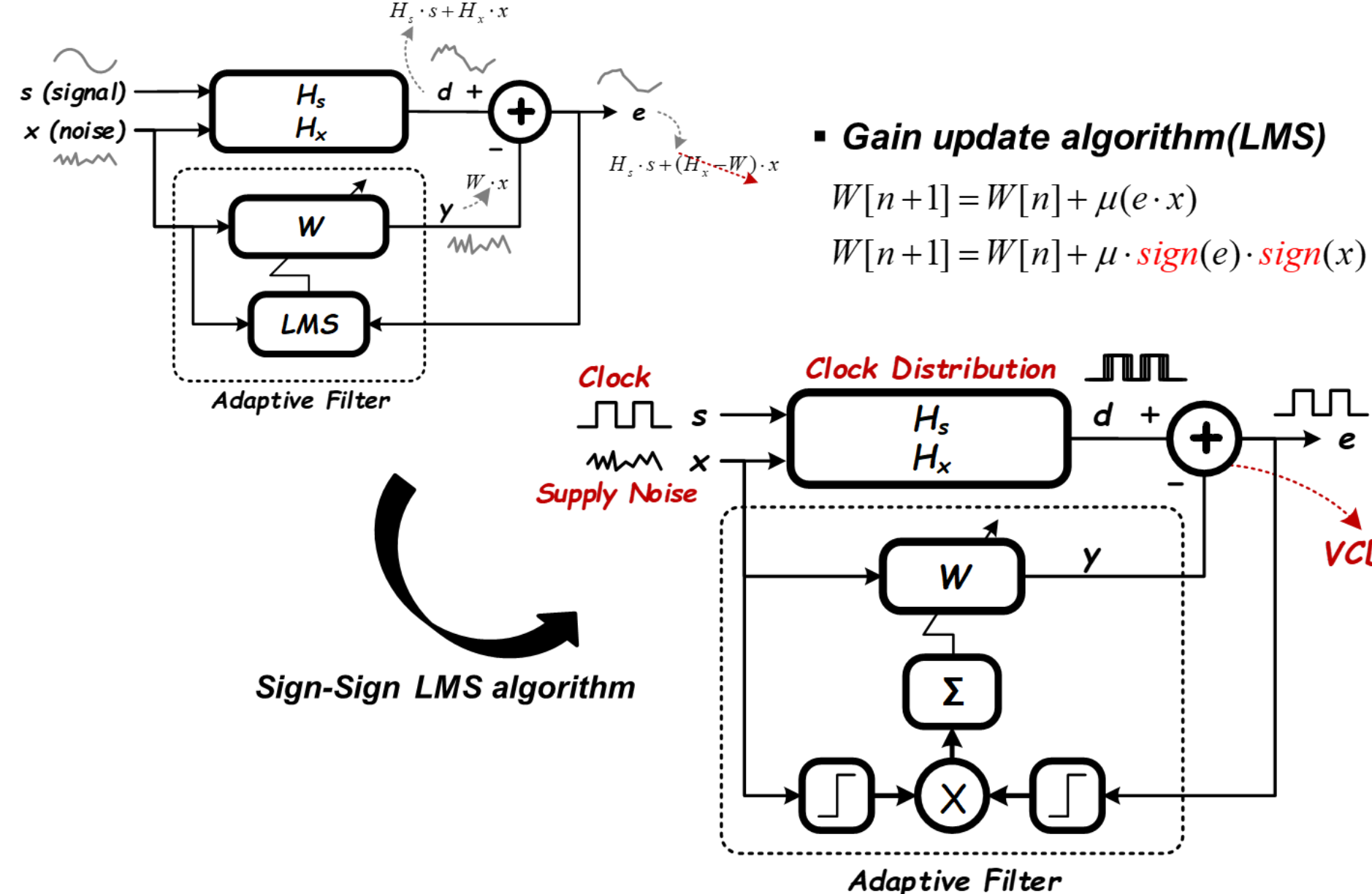
## Jitter Compensation Concept

### Jitter Compensation Concept in Clock Distribution & TX

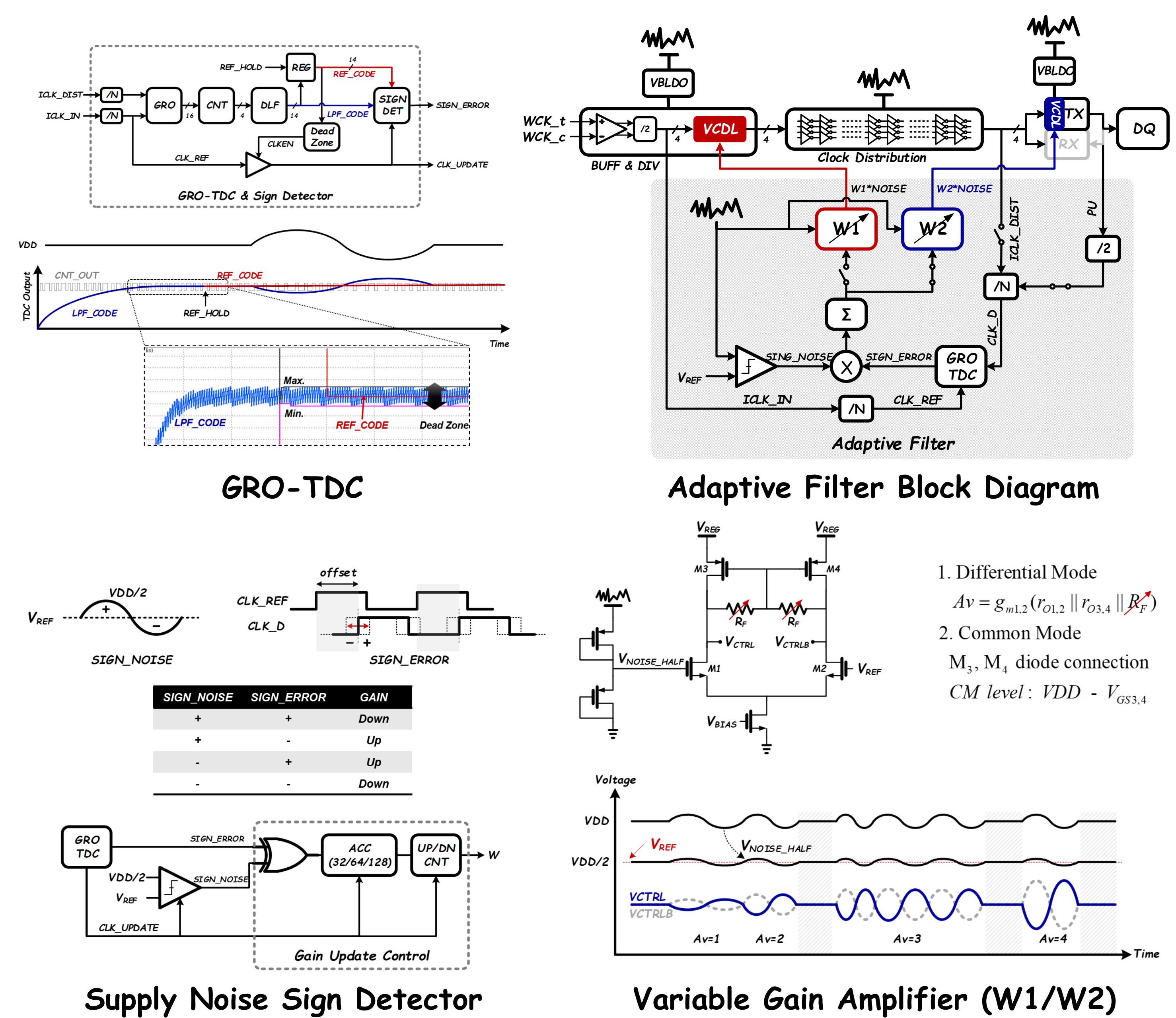
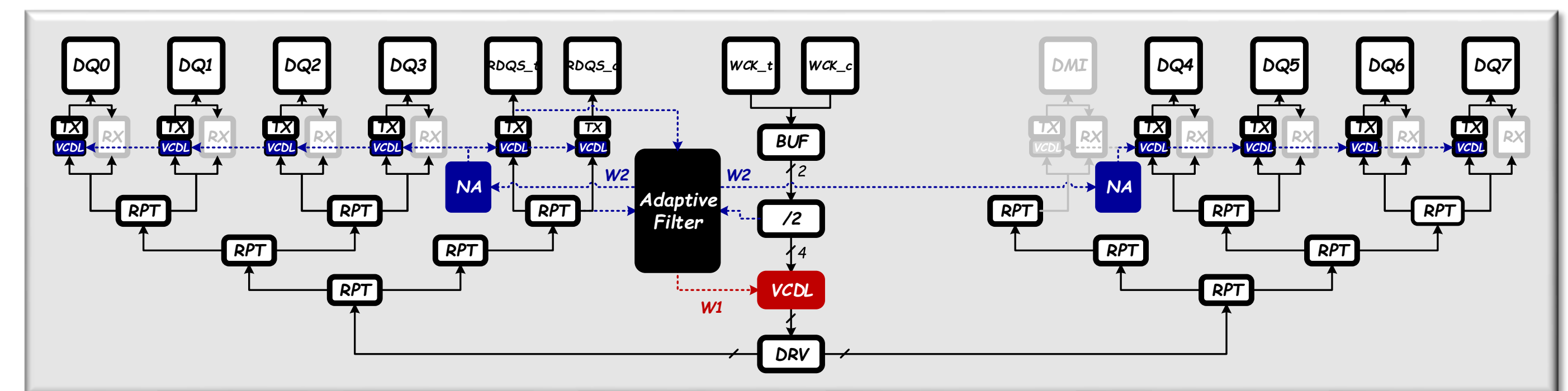


### Adaptive Filter for Gain Calibration

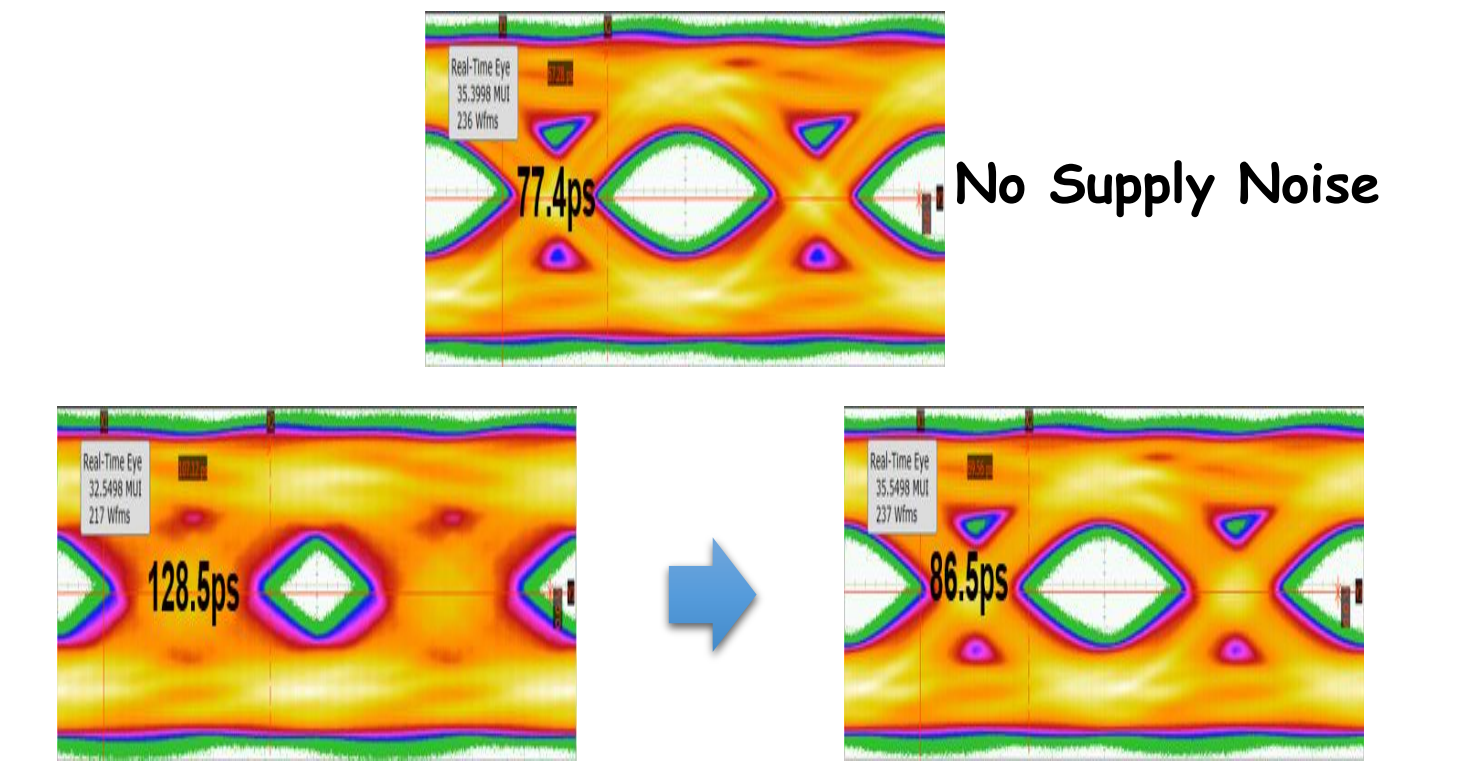
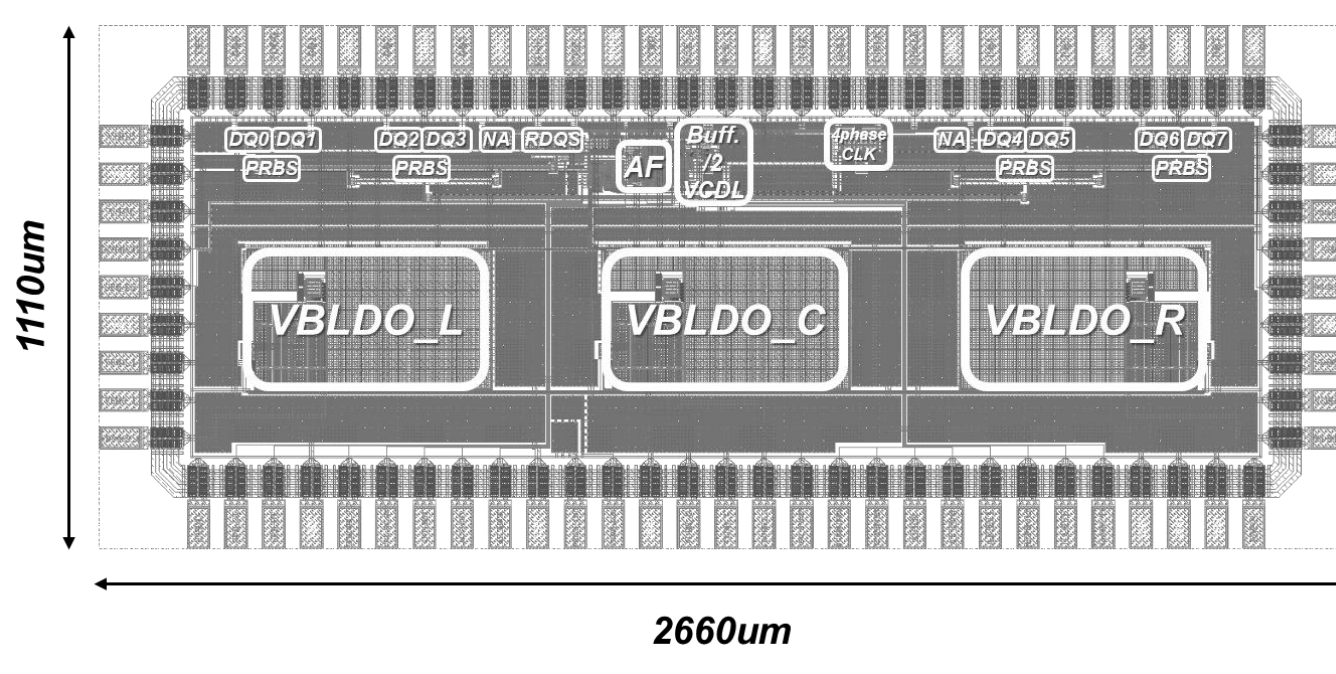
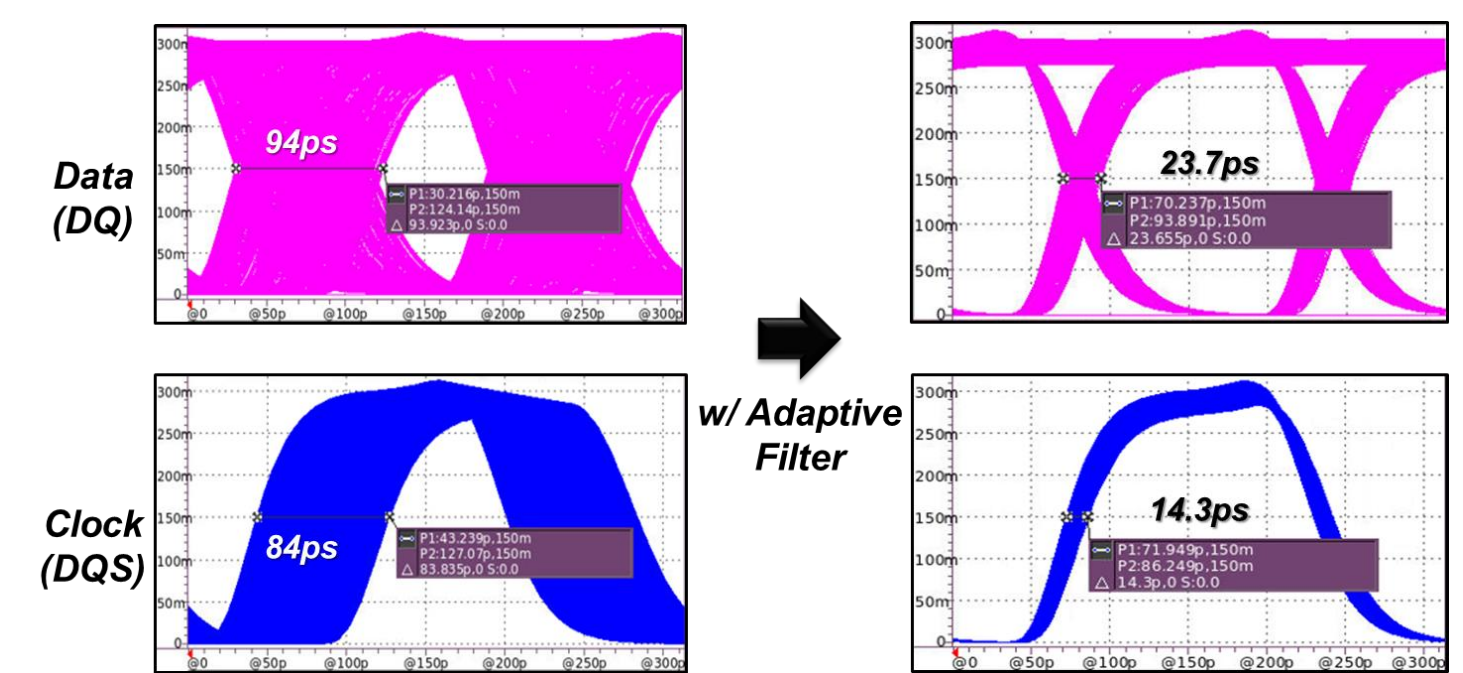
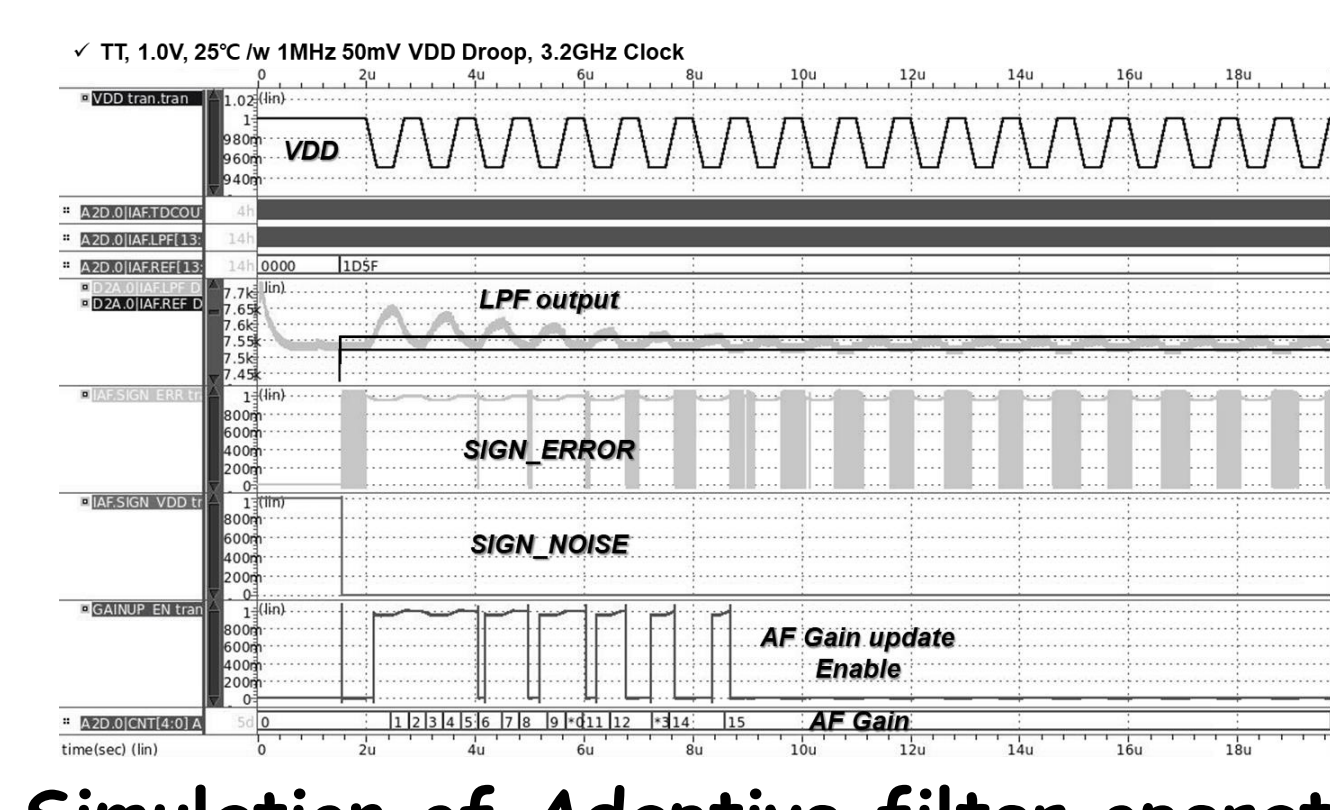
[B. Widrow, Proc. IEEE, 1975]



## Proposed Architecture & Implementation



## Simulation & Measurement Results



Measurement Result @ 6Gbps w/ 1MHz 50mV sine noise

Due to some errors, the gain calibration of the adaptive filter did not work correctly. So, jitter of data and clock was measured by manually calibrating the gain of the adaptive filter through the test mode.

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